AN204

Application Note

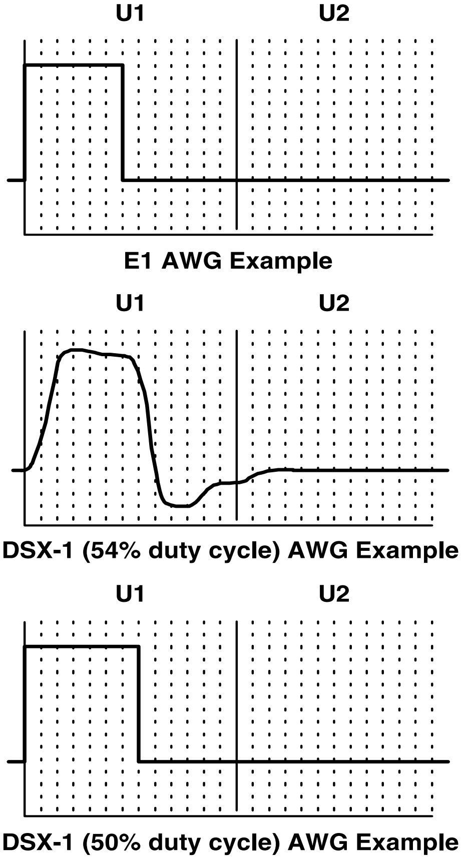
HOW TO USE THE CS61880/CS61884 ARBITRARY WAVEFORM GENERATOR

1. INTRODUCTION

This application note describes how to use the CS61880 and CS61884 Arbitrary Waveform Generator(AWG) function. Using this function allows the user to customize the transmit pulse shapes to compensate for nonstandard cables, transformers, protection circuitry, or to reduce power consumption by reducing the output pulse amplitude. A channel is configured for a custom pulse shape by enabling the AWG for the desired channel and then storing data representing the pulse shape into the phase sample locations of that channel. Each channel has a separate AWG, so all eight channels can have a different customized pulse shape.

Note: The AWG function is only available in host mode.

In the AWG RAM, the pulse shape is divided into two unit intervals (UI). Each UI consists of 12, 13 or 14 phase sample addresses or phase sample index. Table 1 shows the number of phase samples per UI for each different LEN[3:0] settings. The first UI is for the “main” part of the pulse and the second UI is for the “tail” of the pulse (Refer to Figure 1). Thus, a complete pulse-shape is represented by 24, 26 or 28 phase samples. The data in each phase sample is a 7-bit two’s-complement number with a maximum positive value of 0x3f, and a maximum negative value of 0x40. The terms “positive” and “negative” are defined for a positive going pulse only. The pulse generation circuitry automatically inverts the pulse for negative going pulses. The data stored in the lowest phase address corresponds to the first phase sample that will be transmitted in time. The CS61880/884 AWG typical output voltage step size for each mode of operation isas follows: for E1 75 Ω mode the typical voltage step is 42 mV/LSB, for E1 120 Ω mode the typical voltage step is 54 mV/LSB and for all T1 100 Ω modes the typical voltage step is 85 mV/LSB all voltage steps are measured across the transformer secondary.



E1 AWG Example

DSX-1 (54% duty cycle) AWG Example

DSX-1 (50% duty cycle) AWG Example

Figure 1. Arbitrary Waveform UIs

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2. ROM ACCESS

The fastest way to arrive at an ideal pulse shape is to start with one of the pulse shapes which already exists in ROM. The following steps are required to read data from ROM.

1) Set the LEN [3:0] bits in the Line Length Data Register (11h) for the desired channel to match the impedance and line length conditions that are closest to the given application. Refer to the CS61880 or CS61884 data sheets for LEN settings.

2) Make sure that the bits in the AWG Enable Register (19h) corresponding to the desired channels are set to "0" (for example, bit 0 is channel 0, and bit 3 is channel 3). Setting the bits in this register to "1" will access the RAM, not the ROM.

3) Write the desired channel address and phase sample index in the AWG Phase Address Register (17h). Examples of a channel address and phase sample index are shown in Table 2 on page 4. Table 1 shows the number of phase samples per UI for each different LEN[3:0] settings.

Table 1. Phase Samples Per UI vs LEN Settings

LEN[3:0]	Operation Mode	Phase Samples Per UI
0000	E1 120 Ω 3.0 V	12
0001	T1/J1 100 Ω DS1, Option A (undershoot)	14
0010	T1/J1 100 Ω DS1, Option A (0 dB)	14
0011	T1/J1 100 Ω 0 - 133 Ft	13
0100	T1/J1 100 Ω 133 - 266 Ft	13
0101	T1/J1 100 Ω 266 - 399 Ft	13
0110	T1/J1 100 Ω 399- 533 Ft	13
0111	T1/J1 100 Ω 533- 655 Ft	13
1000	E1 75 Ω 2.37 V	12

4) After the channel address and phase sample index have been written, the data from the selected ROM phase sample address is read from the AWG Phase Data Register (18h). This data is a 7-bit two's-complement number with a maximum positive value of 0x3f, and a maximum negative value of 0x40. There are examples of the AWG phase data in Table 3 on page 4.

5) To read the ROM data from a different channel address and/or phase sample index repeat steps 3 and 4 with a different channel address or phase sample index.

Note: The Auto-Increment function can be used to increment the phase sample addresses of the ROM (Refer to Auto-Increment Function (See Section 3.1 on page 3) for more information on this function.).

3. AWG RAM ACCESS

The following steps are required in order to access the RAM data to implement a customized pulse shape.

1) Set the LEN [3:0] bits in the Line Length Data Register (11h) for the desired channels to match the impedance and line length conditions that are closest to the given application. The LEN settings select the number of phase sample indexs in each UI from 12, 13 or 14. Table 1 shows the number of phase samples per UI for each LEN[3:0] setting.

2) The AWG function must be enabled for each desired channel. This is accomplished by writing a "1" to the corresponding bit in the AWG Enable Register (19h) (for example, bit 0 is channel 0, and bit 3 is channel 3). When the corresponding bit in the AWG Enable Register (19h) is set to "0", the AWG function is disabled and the pre-programmed pulse shapes in ROM are selected for transmission, as chosen by the LEN[3:0] settings.

3) Write the desired channel address and phase sample index in the AWG Phase Address Register (17h). Examples of a channel address and phase sample index are shown in Table 2 on page 4. Table 1 shows the number of phase

samples per UI for each LEN[3:0] setting. When the mode of operation calls for only 24- or 26-phase samples. The phase samples that are not used (25 through 28) are ignored and do not effect the shape of the customized pulse shape. To change the phase sample index the user may use either of the following steps. The user can write the new phase sample index along with the channel address to the AWG Phase Address Register (17h). Alternatively, the auto-increment function, which is accessed through bit 7 of the Global Control Register (0Fh), can be used to automatically increment the phase sample index. Refer to the Auto-Increment Function section below for more details.

4) Once the channel address and phase sample index have been written to the AWG Phase Address Register (17h), then the actual phase sample data may be written to or read from the AWG Phase Data Register (18h). There are examples of the AWG phase data in Table 3 on page 4.

Note: When the CS61880 and CS61884 devices are configured for any E1 mode the phase data written to the second UI must be set to zero. Writing any other phase data to the second UI will cause the transmitted pulse shape to be invalid. Also, during E1 mode a negative value is not valid in the first UI.

3.1 Auto-Increment Function

If sequential AWG accesses are to be made, the Auto-Increment function can be used to enable automatic incrementing of the phase sample index. The channel address, however, remains unaffected by the Auto-Increment bit. Since the number of phase samples per UI (12/13/14) varies with the mode of operation, the AWG Address Register (17h) needs to be re-written in order to restart the phase sample index sequence.

Note:: When using the auto-increment function the phase sample index can start from any address.

When bit 7 in the Global Control Register (0Fh) is set to “1” only the first phase sample index (00000 binary) along with the channel address needs to be written to the AWG Phase Address Register (17h). Each subsequent access (write or read) to the AWG Phase Data Register (18h) will automatically increment the phase sample index. Writing to the AWG Phase Adrress Register(17h) re-starts the sequence from the new phase sample index.

Note: The Auto-Increment bit must be set to “1” before the phase sample data is written to or read from the AWG Phase Data Register (18h) to properly increment the phase sample index.

3.2 AWG Broadcast Function

The AWG Broadcast function allows the same phase data to be written to multiple channels simultaneously. This function only requires that one of the eight channel addresses be written to the AWG Phase Address Register (17h). This function is implemented through AWG Broadcast Register(16h). Each bit in the AWG Broadcast Register corresponds to a channel address (for example, bit 0 is channel 0, and bit 3 is channel 3).

Note: This function is disabled when MCLK is not present. Also, the Auto-Increment function can be used in conjunction with the AWG Broadcast function to automatically increment the phase sample index.

The following steps show how to write the same phase sample data to multiple channels.

1) Select the channel or channels by setting the corresponding bit or bits to “1” in the AWG Broadcast Register (16h) of the desired channel or channels.

2) Enable RAM access by writing a “1” to the bits in the AWG Enable Register (19h).

3) Write the channel address and phase sample address to the AWG Phase Address Register (17h) for any channel.

Note: Any channel can be used.

4) Write the phase sample data to the AWG Phase Data Register (18h). The data written to the AWG Phase Data Register (18h) will be written simultaneously to all channels selected by the AWG Broadcast Register (16h) and the channel accessed in the AWG Phase Address Register(17h). If no bits are set to “1” in the AWG Broadcast Register, then only the channel selected by the AWG Phase Address Register is accessed.

Note:: During an AWG read sequence the bits in the AWG Broadcast Register are ignored. The appropriate bits in the AWG Broadcast Register must be set before writing to the AWG Phase Data Register (18h) in order to broadcast write the phase sample data correctly.

4. AWG OVERFLOW REGISTERS

An AWG overflow occurs when invalid phase data is entered, such that a sample-by-sample addition of UI0 and UI1 results in values that exceed the arithmetic range of the 7-bit representation. The AWG Overflow Interrupt Enable Register (1Ah) enables changes in the AWG overflow status to be reflected in the AWG Overflow Interrupt Status Register (1Bh), thus causing an interrupt on the $\overline{\text{INT}}$ pin. The AWG Overflow Interrupt Status Register (1Bh) indicates a change in status of the AWG overflow. Reading the AWG Interrupt Status register clears the interrupt, which deactivates the $\overline{\text{INT}}$ pin.

Table 2. AWG Channel Address and Phase Address Examples

Channel/Phase Address Selected	Channel Address [2:0]			Phase Address [4:0]				
Channel #1 and Phase Address 11	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	0	0	1	0	1	0	1	1
Channel #6 and Phase Address 24	1	1	0	1	1	0	0	0

Table 3. AWG Phase Data Examples

Phase Data Written	RSVD	AWG Phase Data [6:0]						
40h	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	0	1	0	0	0	0	0	0
3Fh	0	0	1	1	1	1	1	1

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